REMARKS

Claims 1-29 are now pending in this application. By this response to the non-final Office Action dated May 15, 2006, claims 27-29 are amended. Care has been taken to avoid the introduction of new matter. Favorable reconsideration of the application in light of the following comments is respectfully solicited.

Objections Under 35 U.S.C. § 101

In section 4 of the Office Action, claims 27-29 are rejected under 35 U.S.C. § 101 for being directed to non-statutory subject matter. In response, Applicant has amended the claims, and respectfully requests withdrawal of the rejection.

Rejections Under 35 U.S.C. § 102(e)

In section 6 of the Office Action, claims 1-3, 7-10, 12, 14, 16-19, 21, 23, 25-26, and 29 are rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6.725,357 (hereinafter "Cousin"). Applicant respectfully traverses the rejection.

Cousin teaches a pipelined computer system that supports three different instruction modes, as is selected by a process status register PSR (*see* col. 3, lines 19-23). Upon *each machine cycle*, the align stage supplies the decoder with a block of 2 or 4 instructions consisting of either: two 16 bit instructions ("GP16 superscaler mode"), two 32 bit instructions ("GP32 superscaler mode"), or four 32 bit instructions ("VLIW mode") (*see* col. 4, lines 24-46; Fig. 1). "Fig. 2 illustrates [the] three different instruction modes" (*see* col. 2, line 62). The decoder supplies each of the instructions via respective channels slot 0 to slot 3 to the subsequent dispatch stage (*see* col. 4, lines 47-50; Fig. 2). In the dispatch stage, one of two things happens upon *each machine cycle*: (1) in GP16 and GP32 modes, the decoded instruction in slot 0 generates micro-instructions in one or both μ slot 0's, and slot 1 generates micro-instructions in

one or both μ slot 1's, for a total of 2-4 micro-instructions generated from a single instruction packet (*see* col. 4, lines 56-64); or (2) in VLIW mode, all 4 μ slots are filled by respective instructions in slots 0-3 (*see* col. 4, line 65 to col. 5, line 13). Of a pair of micro-instructions placed into μ slots 0 and 1 of A-IDQ, at most only one of them may be for the general unit GU (*see* col. 6, lines 32-34). Additionally, the micro-instructions issued from a single instruction packet proceed through the pipeline so as all of the micro-instructions reach their respective execution units on the same machine cycle.

This means that of the micro-instructions issued from an instruction packet, at most one may be a control instruction directed to the general unit GU. As up to only one instruction per instruction packet may be a control instruction, Cousin does not teach the instruction packet(s) which comprise or define a plurality of control instructions, as recited by the claims. In the absence of such packets, it is further unable to execute a plurality of control instructions comprising an instruction packet in sequential or program order, as recited in the claims. Therefore, Cousin does not anticipate the claims under 35 U.S.C. § 102(b).

By contrast, claim 1 recites an "instruction packet [which] defines (i) a plurality of control instructions . . . [and] said control instructions are supplied to the first processing channel for execution in program order." Claim 26 recites an "instruction packet [which] comprises a plurality of control instructions suppl[ied] . . . to said first processing channel for execution in sequence." Claim 29 recites "instruction packets each comprising a plurality of control instructions for execution sequentially." The Office Action does not provide specific support with regard to how the computer system in Cousin is capable of executing a plurality of control instructions within a single instruction packet "sequentially" or "in program order," and Applicant finds no support for such a contention.

Furthermore, claims 1 and 26 recite that "the decode unit detects that the instruction packet comprises a plurality of control instructions." In Cousin, no such detection is performed by the decoder. Rather than the decoder inspecting instruction packets to determine the type and number of instructions in a packet, there is an instruction mode held in a process status register which controls the prefetch buffer and decoder (*see* col. 3, lines 21-25). Furthermore, any "detection" capable of discriminating between control and non-control instructions is performed subsequent to the decode stage by the micro-instruction generator 10. The micro-instruction generator is responsible for issuing micro-instructions, routing them to either the data units or the address/general units in response to instructions presented in slots 0 to 3 (*see* col. 4 line 56 to col. 5, line 13). Thus, Cousin teaches a decoder that does not fulfill the limitations recited in the claims. Therefore, Cousin does not anticipate claims 1 and 26 under 35 U.S.C. § 102(b).

In summary, it has been shown that Cousin does not anticipate claim 1, 26, or 29 under 35 U.S.C. § 102(b). Neither does Cousin anticipate claims 2-25 and 27-28, which depend on claim 1 or 26.

Rejections Under 35 U.S.C. § 103(a)

In section 43 of the Office Action, claims 4-5 and 11 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Cousin in view of U.S. Patent No. 6,880,150 (hereinafter "Takayama"). In section 58 of the Office Action, claims 6, 22, and 24 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Cousin. In section 71 of the Office Action, claims 13 and 15 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Cousin in view of U.S. Patent No. 5,956,518 (hereinafter "DeHon"). In section 82 of the Office Action, claim 20 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Cousin in view of Simonen et al. ("Variable Length Instruction Compression for Area Minimization", Piia Simonen, Ilkka

Saastamoinen, Jari Nurmi, 2003, IEEE; hereinafter "Simonen"). In section 89 of the Office Action, claims 27 and 28 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Cousin in view of Tanenbaum (Andrew S. Tanenbaum. Structured Computer Organization, 1984. pp. 10-11; hereinafter "Tanenbaum"). Applicant respectfully traverses the rejections.

For the reasons discussed with reference to the rejection of independent claims 1 and 26 under 35 U.S.C. § 102(e), Cousin does not teach or suggest a decode unit that detects if an instruction packet defines (i) a plurality of control instructions or (ii) a plurality of instructions one or more of which is a data processing instruction, wherein the control instructions in an instruction packet comprising a plurality of control instructions are supplied to the first processing channel in sequence or program order, as recited by independent claims 1 and 26. The various combinations of references proposed in the Office Action do not remedy the shortcomings of Cousin so as to motivate an artisan to modify the teachings of Cousin to produce what is claimed, and therefore are insufficient to support a rejection under 35 U.S.C. § 103(a).

More specifically, with respect to claims 4, 5, and 11, Takayama is applied for its teaching of "instructions whose word length is not an integer number of bytes" (col. 2, lines 10-11), instructions with a length of 21 bits (col. 13, lines 30-34), and data processing operations with a bit width greater than the bit width for control instructions (col. 13, lines 30-34). Combining such concepts with the teachings of Cousin does not render the claims obvious, as Cousin does not teach a "decode unit . . . operable to . . . [detect] that [an] instruction packet comprises a plurality of control instructions [which] are supplied to the first processing channel for execution in program order," as recited in the parent claim 1. The same claim limitations are incorporated into dependent claims 4, 5, and 11. Additionally, there are significant architectural differences between the two teachings (*compare* Cousin Fig. 2 *with* Takayama Fig. 6), in terms

of pipelining and functional units, that would not motivate or necessarily be within the skill of an artisan to combine the two to produce what is recited in claims 4, 5, and 11.

With respect to claims 6, 22, and 24, the Office Action asserts that it is obvious to modify the length of an instruction packet, modify the bit length of an instruction, and enable a processor to support higher level languages (¶¶ 62, 66, 70). However, Cousin does not teach or suggest a "decode unit . . . operable to . . . [detect] that [an] instruction packet comprises a plurality of control instructions [which] are supplied to the first processing channel for execution in program order," as recited in the parent claim 1. The proposed modifications do not remedy the shortcomings of Cousin. The same claim limitations are incorporated into dependent claims 6, 22, and 24. Therefore, these claims are not unpatentable in view of Cousin.

With respect to claims 13 and 15, DeHon is applied for its teaching of a reconfigurable mesh/array of basic functional unit (BFU) cores which may be reconfigured so as to enable the array to function as or emulate a SIMD and/or VLIW system (*see, e.g*, col. 5, lines 24-27 and 44-45). However flexible such a reconfigurable system may be, the reference supplies no teachings related to a "decode unit . . . operable to . . . [detect] that [an] instruction packet comprises a plurality of control instructions [which] are supplied to the first processing channel for execution in program order," as recited in the parent claim 1, and neither taught nor suggested by Cousin. Cousin and DeHon, alone or in combination, do not teach, suggest, or motivate an artisan to modify the teachings of Cousin so as to produce the limitations recited in claim 1, which are incorporated into its dependent claims 13 and 15.

With respect to claim 20, Simonen is applied for its teaching of "instructions [which] were expanded to 34 bits" (§ 3.1). Simonen further discusses a method for compressing DSP instructions, and some of the benefits achieved thereby. However, the reference supplies no

teachings related to a "decode unit . . . operable to . . . [detect] that [an] instruction packet comprises a plurality of control instructions [which] are supplied to the first processing channel for execution in program order," as recited in the parent claim 1, and neither taught nor suggested by Cousin. Cousin and Simonen, alone or in combination, do not teach, suggest, or motivate an artisan to modify the teachings of Cousin so as to produce the limitations recited in claim 1, which are incorporated into its dependent claim 20.

With respect to claims 27 and 28, Tanenbaum is applied for its teaching of the proposition that "hardware and software are logically equivalent." The Office Action applies the reference in the sense that "the method disclosed in [claims 27 and 28 may be implemented] in software as opposed to hardware" (¶¶ 93, 97). However, the Tanenbaum reference supplies no teachings regarding the functioning of a decode unit within a computer processor, nor a "decode unit [that] detects that [an] instruction packet comprises a plurality of control instructions [and supplies] said plurality of control instructions to [a] first processing channel for execution in sequence," as recited in the parent claim 26, and neither taught nor suggested by Cousin. Cousin and Tanenbaum, alone or in combination, do not teach, suggest, or motivate an artisan to modify the teachings of Cousin so as to produce the limitations recited in claim 26, which are incorporated into its dependent claims 28 and 29.

In summary, it has been shown that none of the proposed combinations of references cure the shortcomings of Cousin. Therefore, the claims are patentable under 35 U.S.C. § 103(a), even in view of the cited references.

For the above reasons, Applicant believes that the application is in condition for allowance. Applicant respectfully requests the Examiner's favorable consideration as to allowance. The Examiner is invited to contact the Applicant's representative listed below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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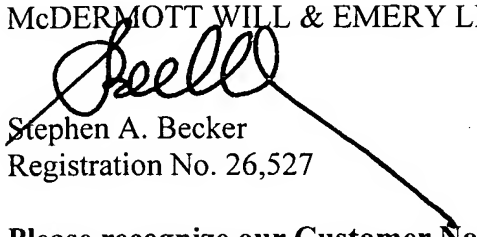

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